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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/073,316	02/13/2002	Hideo Nunokawa	020101	5321

23850 7590 01/16/2003

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EXAMINER
VU, QUANG D

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 01/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/073,316	NUNOKAWA, HIDEO	
	Examiner	Art Unit	
	Quang D Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,677,570 to Kondoh et al. in view of US Patent No. 6,328,176 to Zivic.

Regarding claim 1, Kondoh et al. (figures 2, 3A-B) teach a semiconductor device comprising:

a semiconductor chip (5) having a circuit block, a power supply line and a ground line; and

Kondoh et al. differ from the claimed invention by not showing the condenser chip is stacked on the semiconductor chip. However, Zivic (figures 1-4) teaches the condenser chip (2) is stacked on the semiconductor chip (1). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the condenser chip is stacked on the semiconductor chip of Zivic into the device taught by Kondoh et al. because it can save the space of the semiconductor substrate.

It is inherent that a condenser chip in which a noise reduction condenser connected to the circuit block is formed.

Regarding claim 2, Kondoh et al. teach a plurality of circuit blocks are formed in the semiconductor chip, and the condenser chip has a plurality of condensers corresponding to the circuit blocks.

Regarding claim 3, Kondoh et al. teach a plurality of circuit blocks are formed in the semiconductor chip, and a plurality of the condenser chips are provided corresponding to the circuit blocks.

Regarding claim 4, Kondoh et al. teach the semiconductor chip (5) has a first power supply pad (6a) provided on a connecting line extending from one of the power supply line (3a) and the ground line (2a) to the circuit block; and

the condenser chip (7b) has a second electrode pad (6b) connected to the condenser, and the second electrode pad of the condenser chip is electrically connected to the first electrode pad (6a) of the semiconductor chip (5) through a bonding wire.

Regarding claim 5, Kondoh et al. teach the semiconductor chip (5) has a first power supply pad (6a) provided on a connecting line extending from one of the power supply line (3a) and the ground line (2a) to the circuit block; and

the condenser chip (7b) has a second electrode pad (6b) connected to the condenser, and the condenser chip (7b) is connected to the first electrode pad (6a) of the semiconductor chip (5).

Regarding claim 6, Kondoh et al. and Zivic do not teach the noise reduction condenser of the condenser chip is formed by a MOS capacity. It would have been obvious to one having ordinary skill in the art at the time the invention was made to reduce noise, since the noise can be reduced by the condenser chip.

Regarding claim 7, Kondoh et al. teach the semiconductor chip (5) has a third electrode pad (6c) other than the first electrode pad (6a) connected to the circuit block;

The condenser chip has a fourth electrode pad (6d) other than the second electrode pad (6b) connected to the condenser; and

an inductor connected to at least one of the power line (3a) and the ground line (2a) if formed by connecting the fourth electrode pad of the condenser chip and the third electrode pad of the semiconductor chip (5) by a bonding wire.

Regarding claim 8, Kondoh et al. teach a fourth electrode pad (6d) of the condenser chip are provided and a the third electrode pad (6c) of the semiconductor chip are provided; and

the inductor is formed by alternately and sequentially connecting the fourth electrode pads of the condenser chip and the third electrode pads of the semiconductor chip by bonding wires.

Regarding claim 9, Kondoh et al. teach a semiconductor device comprising:

a first semiconductor chip (5) having a circuit block, a power supply line (3a) and a ground line (2a); wherein the first semiconductor chip (5) has a first electrode pad (6a) separated form a circuit formed within the first semiconductor chip (5);

an inductor connected to at least one of the power line and the ground line is formed by connecting the first electrode pad of the first semiconductor chip.

Kondoh et al. differ from the claimed invention by not showing a second semiconductor chip stacked on the first semiconductor chip. The plurality of structures being stacked such that each such structure but one is on top of another such structure such that the plurality of structure thereby form a multiplayer composite structure. It has been held that mere duplication of parts has no patentable significance unless a new and unexpected result is produced.

Regarding claim 10, Kondoh et al. teach the first electrode pad of the first semiconductor chip are provided; and

the inductor is formed by alternately and sequentially connecting the first electrode pad of the first semiconductor chip.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 703-305-3826. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

qv
January 8, 2003

Sara Crane
Primary Examiner